Agilent E9520A Inverse Assembler for the MPC85xx

Design Guide

Agilent Technologies

Notices

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1 Introduction

In This Guide...

This *Design Guide* provides information to assist you in designing a board which will be compatible with the Agilent E9520A Inverse Assembler for the MPC85xx. It tells you what signals are required by the decoder, and suggests how to route these signals to a connector.

For information on using the decoder, see the online help which is installed with the decoder.

Product Overview

The Agilent E9520A Inverse Assembler for the Motorola MPC8540 and MPC8560 simplifies debug by disassembling instruction fetches into PowerQUICC III mnemonics. Support is provided for both the Local Bus General Purpose Chip Select Machine (GPCM) and for the DDR Bus. The inverse assembler supports cache-on trace. Connection to the analyzer may be made using Mictor connectors, Samtec connectors, soft touch connectorless probing, or a FuturePlus analysis probe.

Target System Requirements

The inverse assembler has been designed to work with target systems meeting the following requirements:

Supported processor

- Freescale Semiconductor's MPC8540 and MPC8560 processor with a GPCM or DDR bus.

Object files

- For cache-on tracing, you must have access to the object files for the code which is executing on your target system.
- You must know the memory address where the object code is loaded.

Supported compilers

- Any compiler which generates statically linked object files in the standard ELF format.

Connectors

You must provide a way to connect logic analyzer probes to the signals on your target system.

- You can route the required signals from the processor to connectors, as described in this manual, or
- For SDRAM memory, you can use one of the following analysis probes:
  - FuturePlus FS2331 DDR SDRAM analysis probe
  - FuturePlus FS2333 SODIMM DDR analysis probe
  - FuturePlus FS2336 DDR400 DIMM basic analysis probe/interposer

Equipment Required

Logic analysis system

You need an Agilent 16900-series or 1680/90-series logic analyzer.

Logic analyzer cards

The logic analyzer card(s) you use must support the speed of the bus you are probing.

The logic analyzer card(s) must provide enough channels to probe the connectors on your target system.

Table 1 Logic analyzer cards required

Probing scheme	Number of connectors	Number of logic analyzer channels required	Number of 68-channel logic analyzer cards
GPCM Multiplexed	2 3	68 (no parity) 102 (with parity)	1 2
GPCM Demultiplexed	3 4	102 (no parity) 136 (with parity)	2 2
DDR	4	272 (see explanation)	4

Explanation: why DDR requires extra channels

DDR requires 272 channels. One might expect that four connectors would require 136 logic analyzer channels. The extra channels are required for two reasons:

- For three of the connectors, each signal is sampled twice on each clock edge—once with a sample position appropriate for data reads, and again with a sample position appropriate for data writes. Therefore, two logic analyzer channels are mapped to each signal.

- Depending on the speed of the logic analyzer card and the speed of the DDR clock, it may be necessary to run the logic analyzer in “turbo” mode. In this case, an extra 34 logic analyzer channels must be left unconnected, so that they can be used to store time stamps.

Probes

You need an appropriate number of logic analyzer probes (“adapter cables”) to connect the logic analyzer cables to the connectors on your target system. You need one probe for each connector. The probe must match the type of connector you have placed on your board. For GPCM, Agilent recommends MICTOR connectors and Agilent E5346A or E5380A MICTOR probes. For DDR, Agilent recommends soft touch pads and E5394A or E5390A soft touch connectorless probes.

2
Designing Your Board (GPCM)

This chapter describes the factors you need to consider when designing and preparing your target system for logic analysis.

Overview of the Connectors

You must provide two, three, or four AMP MICTOR 38 connectors with the signal mappings shown in the following sections, or other connectors which map the signals to the same logic analyzer channels.

Designing the Connectors

AMP MICTOR 38 connectors

The signal-to-connector mappings shown in this chapter assume you are using AMP MICTOR 38 connectors.

Each MICTOR 38 connector carries 32 signals plus two clocks (CLK1 for two logic analyzer pods). Probes (part number E5346A, sometimes called “high-density termination cables”) are required to connect the logic analyzer cables to the MICTOR connector. These probes contain the required termination. One probe is required for every two logic analyzer pods.

To increase the structural support for the probes, you should use support shrouds on each connector.

For more information, including mechanical dimensions, see the *Agilent Technologies E5346A 38-Pin Probe and E5351A 38-Pin Adapter Cable Installation Note*, available from www.agilent.com.

Design Considerations

The connector must be close enough to the signal source so that the stub length created is less than $^{1}/_{5}$ the t_r (bus risetime). For PC board material, (er = 4.9) and Z_o in the range of 50 - 80Ω, use a propagation delay of 160 ps/inch of stub.

Each probed signal line must be able to supply a minimum of 600 mV to the probe tip and handle a minimum of 90 kΩ shunted by 10 pF. The maximum input voltage to the logic analyzer is ±40V peak

Other connectors

You may use other connector/probe combinations, including:

- Agilent soft touch connectorless probes
- Agilent pro series soft touch connectorless probes
- Samtec connectors with Agilent Samtec probes

Design information for these connectors can be found on the web at www.agilent.com. If you use one of these connectors, route each signal to the same logic analyzer signal as shown for the MICTOR connector. For example, **LAD[15]** should always be connected to **D0 even** on the logic analyzer, regardless of which connector/probe combination is used.

NOTE

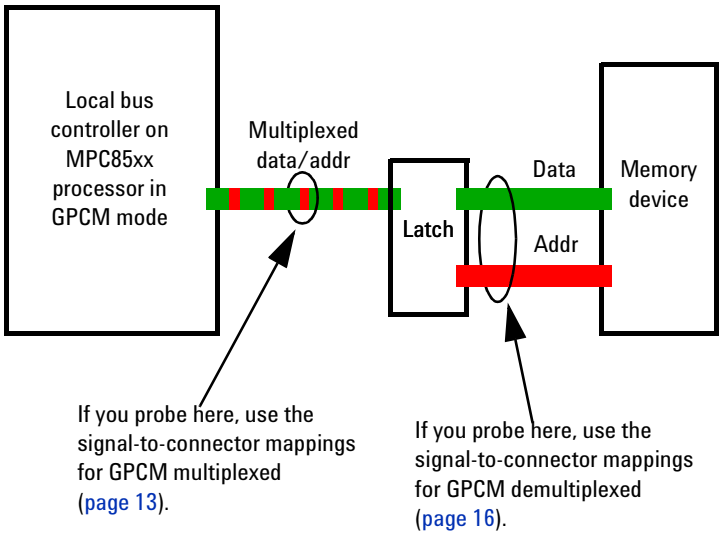
Agilent strongly recommends that you use the signal-to-connector mappings shown in this *Design Guide*. It is possible to use the inverse assembler with your own signal-to-connector mappings. In this case, please keep the following points in mind:

- You must provide all of the signals specified in this Design Guide.
- You will not be able to use the logic analyzer configuration files which are supplied with the inverse assembler. You will need to create your own configuration file.

Multiplexed or demultiplexed?

Data and address signals on the GPCM bus are multiplexed. The signals are typically demultiplexed using a latch near the memory parts. Section 13.4.2 of the *Motorola MPC8240 Integrated Processor Reference Manual* describes how to demultiplex the GPCM bus using a simple latch.

You can probe the multiplexed signals, or you can probe the demultiplexed signals.



Signal-To-Connector Mappings for GPCM multiplexed

J1: Address and data

This connector is required.

Logic Analyzer Pod 2	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 1
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	LCLK[0]	5	6	LALE	CLK odd
D15 even	LAD[0]	7	8	LAD[16]	D15 odd
D14 even	LAD[1]	9	19	LAD[17]	D14 odd
D13 even	LAD[2]	11	12	LAD[18]	D13 odd
D12 even	LAD[3]	13	14	LAD[19]	D12 odd
D11 even	LAD[4]	15	16	LAD[20]	D11 odd
D10 even	LAD[5]	17	18	LAD[21]	D10 odd
D9 even	LAD[6]	19	20	LAD[22]	D9 odd
D8 even	LAD[7]	21	22	LAD[23]	D8 odd
D7 even	LAD[8]	23	24	LAD[24]	D7 odd
D6 even	LAD[9]	25	26	LAD[25]	D6 odd
D5 even	LAD[10]	27	28	LAD[26]	D5 odd
D4 even	LAD[11]	29	30	LAD[27]	D4 odd
D3 even	LAD[12]	31	32	LAD[28]	D3 odd
D2 even	LAD[13]	33	34	LAD[29]	D2 odd
D1 even	LAD[14]	35	36	LAD[30]	D1 odd
D0 even	LAD[15]	37	38	LAD[31]	D0 odd

Bus and signal descriptions for J1

NC Pins 1, 2, 3, and 4 must be true no-connects.

LAD Required.

Address is valid on LALE = 1 and falling LCLK.

Data is valid on MDVAL = 1 and falling LCLK.

J2: Control

This connector is required.

Logic Analyzer Pod 4	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 3
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	user defined	5	6	MDVAL	CLK odd
D15 even	LBCTL	7	8	MSRCID[4]	D15 odd
D14 even	#LWE [3]	9	19	MSRCID[3]	D14 odd
D13 even	#LWE [2]	11	12	MSRCID[2]	D13 odd
D12 even	#LWE [1]	13	14	MSRCID[1]	D12 odd
D11 even	#LWE [0]	15	16	MSRCID[0]	D11 odd
D10 even	LA[27]	17	18	user defined	D10 odd
D9 even	LA[28]	19	20	TRIG_OUT	D9 odd
D8 even	LA[29]	21	22	LCKE	D8 odd
D7 even	LA[30]	23	24	#LCS[7]	D7 odd
D6 even	LA[31]	25	26	#LCS[6]	D6 odd
D5 even	LGPL5	27	28	#LCS[5]	D5 odd
D4 even	LGPL4	29	30	#LCS[4]	D4 odd
D3 even	LGPL3	31	32	#LCS[3]	D3 odd
D2 even	LGPL2	33	34	#LCS[2]	D2 odd
D1 even	LGPL1	35	36	#LCS[1]	D1 odd
D0 even	LGPL0	37	38	#LCS[0]	D0 odd

Bus and signal descriptions for J2

NC Pins 1, 2, 3, and 4 must be true no-connects.

MDVAL Required.

MSRCID Required. To enable the signals, MSRCID0 must be sampled low on POR (power-up, reset).

See the *Motorola MPC8540 Integrated Processor Reference Manual*, section 20.4.3, for information on the required debug signals.

J4: Parity

This connector is optional.

Logic Analyzer Pod 6	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 7
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even		5	6		CLK odd
D15 even		7	8		D15 odd
D14 even		9	19		D14 odd
D13 even		11	12		D13 odd
D12 even		13	14		D12 odd
D11 even		15	16		D11 odd
D10 even		17	18		D10 odd
D9 even		19	20		D9 odd
D8 even		21	22		D8 odd
D7 even		23	24		D7 odd
D6 even		25	26		D6 odd
D5 even		27	28		D5 odd
D4 even		29	30		D4 odd
D3 even		31	32	LDP[3]	D3 odd
D2 even		33	34	LDP[2]	D2 odd
D1 even		35	36	LDP[1]	D1 odd
D0 even		37	38	LDP[0]	D0 odd

Bus and signal descriptions for J4

NC Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.

LDP Optional. Parity bits.

Designing connectors for GPCM demultiplexed

J1: Data

This connector is required.

Logic Analyzer Pod 2	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 1
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	LCLK[0]	5	6	LALE	CLK odd
D15 even	LAD[0]	7	8	LAD[16]	D15 odd
D14 even	LAD[1]	9	10	LAD[17]	D14 odd
D13 even	LAD[2]	11	12	LAD[18]	D13 odd
D12 even	LAD[3]	13	14	LAD[19]	D12 odd
D11 even	LAD4]	15	16	LAD[20]	D11 odd
D10 even	LAD[5]	17	18	LAD[21]	D10 odd
D9 even	LAD[6]	19	20	LAD[22]	D9 odd
D8 even	LAD[7]	21	22	LAD[23]	D8 odd
D7 even	LAD[8]	23	24	LAD[24]	D7 odd
D6 even	LAD[9]	25	26	LAD[25]	D6 odd
D5 even	LAD[10]	27	28	LAD[26]	D5 odd
D4 even	LAD[11]	29	30	LAD[27]	D4 odd
D3 even	LAD[12]	31	32	LAD[28]	D3 odd
D2 even	LAD[13]	33	34	LAD[29]	D2 odd
D1 even	LAD[14]	35	36	LAD[30]	D1 odd
D0 even	LAD[15]	37	38	LAD[31]	D0 odd

Bus and signal descriptions for J1

NC Pins 1, 2, 3, and 4 must be true no-connects.

LAD Required. Both Address (Latched LAD) and Data (LAD) are valid on MDVAL (TA) = 1 and falling LCLK.

J2: Control

This connector is required.

Logic Analyzer Pod 4	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 3
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	user defined	5	6	MDVAL	CLK odd
D15 even	LBCTL	7	8	MSRCID[4]	D15 odd
D14 even	#LWE [3]	9	10	MSRCID[3]	D14 odd
D13 even	#LWE [2]	11	12	MSRCID[2]	D13 odd
D12 even	#LWE [1]	13	14	MSRCID[1]	D12 odd
D11 even	#LWE [0]	15	16	MSRCID[0]	D11 odd
D10 even	LA[27]	17	18	user defined	D10 odd
D9 even	LA[28]	19	20	TRIG_OUT	D9 odd
D8 even	LA[29]	21	22	LCKE	D8 odd
D7 even	LA[30]	23	24	#LCS[7]	D7 odd
D6 even	LA[31]	25	26	#LCS[6]	D6 odd
D5 even	LGPL5	27	28	#LCS[5]	D5 odd
D4 even	LGPL4	29	30	#LCS[4]	D4 odd
D3 even	LGPL3	31	32	#LCS[3]	D3 odd
D2 even	LGPL2	33	34	#LCS[2]	D2 odd
D1 even	LGPL1	35	36	#LCS[1]	D1 odd
D0 even	LGPL0	37	38	#LCS[0]	D0 odd

Bus and signal descriptions for J2

NC Pins 1, 2, 3, and 4 must be true no-connects.

MDVAL Required.

MSRCID Required. To enable the signals, MSRCID0 must be sampled low on POR (power-up, reset).

See the *Motorola MPC8540 Integrated Processor Reference Manual*, section 20.4.3, for information on the required debug signals.

J3: Address

This connector is required.

Logic Analyzer Pod 6	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 5
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even	user defined	5	6	user defined	CLK odd
D15 even	Latched LAD[0]	7	8	Latched LAD[16]	D15 odd
D14 even	Latched LAD[1]	9	10	Latched LAD[17]	D14 odd
D13 even	Latched LAD[2]	11	12	Latched LAD[18]	D13 odd
D12 even	Latched LAD[3]	13	14	Latched LAD[19]	D12 odd
D11 even	Latched LAD[4]	15	16	Latched LAD[20]	D11 odd
D10 even	Latched LAD[5]	17	18	Latched LAD[21]	D10 odd
D9 even	Latched LAD[6]	19	20	Latched LAD[22]	D9 odd
D8 even	Latched LAD[7]	21	22	Latched LAD[23]	D8 odd
D7 even	Latched LAD[8]	23	24	Latched LAD[24]	D7 odd
D6 even	Latched LAD[9]	25	26	Latched LAD[25]	D6 odd
D5 even	Latched LAD[10]	27	28	Latched LAD[26]	D5 odd
D4 even	Latched LAD[11]	29	30	Latched LAD[27]	D4 odd
D3 even	Latched LAD[12]	31	32	Latched LAD[28]	D3 odd
D2 even	Latched LAD[13]	33	34	Latched LAD[29]	D2 odd
D1 even	Latched LAD[14]	35	36	Latched LAD[30]	D1 odd
D0 even	Latched LAD[15]	37	38	Latched LAD[31]	D0 odd

Bus and signal descriptions for J3

NC Pins 1, 2, 3, and 4 must be true no-connects.

LAD Required. Both Address (Latched LAD) and Data (LAD) are valid on MDVAL (TA) =1 and falling LCLK.

J4: Parity

This connector is optional.

Logic Analyzer Pod 6	8560 Signal	Mictor pin #		8560 Signal	Logic Analyzer Pod 7
5V	NC	1	2	NC	I2C
5V	NC	3	4	NC	I2C
CLK even		5	6		CLK odd
D15 even		7	8		D15 odd
D14 even		9	10		D14 odd
D13 even		11	12		D13 odd
D12 even		13	14		D12 odd
D11 even		15	16		D11 odd
D10 even		17	18		D10 odd
D9 even		19	20		D9 odd
D8 even		21	22		D8 odd
D7 even		23	24		D7 odd
D6 even		25	26		D6 odd
D5 even		27	28		D5 odd
D4 even		29	30		D4 odd
D3 even		31	32	LDP[3]	D3 odd
D2 even		33	34	LDP[2]	D2 odd
D1 even		35	36	LDP[1]	D1 odd
D0 even		37	38	LDP[0]	D0 odd

Bus and signal descriptions for J4

NC Pins 1, 2, 3, and 4 must be true no-connects. Other NC signals can be left floating (no connects), or used to measure other signals of interest.

LDP Optional. Parity bits.

3
Designing Your Board (DDR)

This chapter describes the factors you need to consider when designing and preparing your target system for logic analysis.

Overview of the Connectors

You must provide four sets of pads with the signal mappings shown in the following sections for Agilent soft touch connectorless probes, or other connectors which map the signals to the same logic analyzer channels.

Other connectors

You may use other connector/probe combinations. Design information for these connectors can be found on the web at www.agilent.com. If you use one of these connectors, route each signal to the same logic analyzer signal as shown for the connectors in this chapter. For example, the **DQ0** signal should always be connected to **D0 even** on the logic analyzer, regardless of which connector/probe combination is used.

NOTE

Agilent strongly recommends that you use the signal-to-connector mappings shown in this *Design Guide*. It is possible to use the inverse assembler with your own signal-to-connector mappings. In this case, please keep the following points in mind:

- You must provide all of the signals specified in this Design Guide.
- You will not be able to use the logic analyzer configuration files which are supplied with the inverse assembler. You will need to create your own configuration file.
- You must not mix single data rate signals and double data rate signals onn the same half (even or odd) of a connector.

Signal-To-Connector Mappings for Soft Touch Probing

Connector J1: Data (double data rate)

Logic Analyzer		MPC85xx Signal	Soft Touch Pad #		MPC85xx Signal	Logic Analyzer	
	D1	DQ4	A1	B1	DQ0	D0	
	D3	DQ1	A2	B2	DQ5	D2	
	Gnd	Gnd	A3	B3	Gnd	Gnd	
	D5	DM0	A4	B4	DQS0	D4	
	D7	DQ6	A5	B5	DQ2	D6	Pod 1
Pod 1	Gnd	Gnd	A6	B6	Gnd	Gnd	(Odd)
(Odd)	D9	DQ3	A7	B7	DQ7	D8	
	D11	DQ9	A8	B8	DQ8	D10	
	Gnd	Gnd	A9	B9	Gnd	Gnd	
	D13	DQS1	A10	B10	DQ12	D12	
	D15	DM1	A11	B11	DQ13	D14	
	Gnd	Gnd	A12	B12	Gnd	Gnd	
	Clk(-)	No connect	A13	B13	No connect	Clk(+)	
	Gnd	Gnd	A14	B14	Gnd	Gnd	
	D1	DQ15	A15	B15	DQ14	D0	
	D3	DQ11	A16	B16	DQ10	D2	
	Gnd	Gnd	A17	B17	Gnd	Gnd	
	D5	DQ16	A18	B18	DQ20	D4	
	D7	DQS2	A19	B19	DQ17	D6	
Pod 2	Gnd	Gnd	A20	B20	Gnd	Gnd	Pod 2
(Even)	D9	DM2	A21	B21	DQ21	D8	(Even)
	D11	DQ22	A22	B22	DQ18	D10	
	Gnd	Gnd	A23	B23	Gnd	Gnd	
	D13	DQ23	A24	B24	DQ19	D12	
	D15	DQ28	A25	B25	DQ24	D14	
	Gnd	Gnd	A26	B26	Gnd	Gnd	
	Clk(-)	No connect	A27	B27	No connect	Clk(+)	

Bus and signal descriptions for J1

DQ Required.

DM Required.

DQS[0,1,2] Optional

Connector J2: Address and control (single data rate)

Logic Analyzer		MPC85xx Signal	Soft Touch Pad #		MPC85xx Signal	Logic Analyzer	
	D1	No connect	A1	B1	No connect	D0	
	D3	A1	A2	B2	A0	D2	
	Gnd	Gnd	A3	B3	Gnd	Gnd	
	D5	A3	A4	B4	A2	D4	
	D7	A5	A5	B5	A4	D6	Pod 3
Pod 3	Gnd	Gnd	A6	B6	Gnd	Gnd	(Odd)
(Odd)	D9	A7	A7	B7	A6	D8	
	D11	A9	A8	B8	A8	D10	
	Gnd	Gnd	A9	B9	Gnd	Gnd	
	D13	A11	A10	B10	A10	D12	
	D15	A13	A11	B11	A12	D14	
	Gnd	Gnd	A12	B12	Gnd	Gnd	
	Clk(-)	No connect	A13	B13	No connect	Clk(+)	
	Gnd	Gnd	A14	B14	Gnd	Gnd	
	D1	CKE1	A15	B15	#RESET	D0	
	D3	No connect	A16	B16	CKE0	D2	
	Gnd	Gnd	A17	B17	Gnd	Gnd	
	D5	BA0	A18	B18	BA1	D4	
	D7	#WE	A19	B19	#RAS	D6	
Pod 4	Gnd	Gnd	A20	B20	Gnd	Gnd	Pod 4
(Even)	D9	#CS0	A21	B21	#CAS	D8	(Even)
	D11	#CS2	A22	B22	#CS1	D10	
	Gnd	Gnd	A23	B23	Gnd	Gnd	
	D13	No connect	A24	B24	#CS3	D12	
	D15	No connect	A25	B25	No connect	D14	
	Gnd	Gnd	A26	B26	Gnd	Gnd	
	Clk(-)	#CK	A27	B27	CK	Clk(+)	

Bus and signal descriptions for J2

If you change the signal mapping to accommodate your board layout, use this connector for all single data rate signals. All double data rate signals (DQ[0:63], DQS[0:9], DM[0:7], MSCRID, and MDVAL) must be assigned to the three double data rate connectors.

A[0:14] All address lines used by your memory part are required.

BA[0:1] Required.

CK, #CK Required.

#CS[0:3] Required.

WE Required.

Connector J3: Data (double data rate)

Logic Analyzer		MPC85xx Signal	Soft Touch Pad #		MPC85xx Signal	Logic Analyzer	
	D1	DQ25	A1	B1	DM4	D0	
	D3	DQS3			DQ29	D2	
	Gnd	Gnd	A3	B3	Gnd	Gnd	
	D5	DQ26	A4	B4	DM3	D4	
	D7	DQ27	A5	B5	DQ30	D6	Pod 5
Pod 5	Gnd	Gnd	A6	B6	Gnd	Gnd	(Odd)
(Odd)	D9	DQS8 *	A7	B7	DQ31	D8	
	D11	DQ32	A8	B8	DM8	D10	
	Gnd	Gnd	A9	B9	Gnd	Gnd	
	D13	DQ33	A10	B10	DQ36	D12	
	D15	DQS4	A11	B11	DQ37	D14	
	Gnd	Gnd	A12	B12	Gnd	Gnd	
	Clk(-)	Gnd	A13	B13	DQ34	Clk(+)	
	Gnd	Gnd	A14	B14	Gnd	Gnd	
	D1	DQ39	A15	B15	DQ38	D0	
	D3	DQ40	A16	B16	DQ35	D2	
	Gnd	Gnd	A17	B17	Gnd	Gnd	
	D5	DQ45	A18	B18	DQ44	D4	
	D7	DQS5	A19	B19	DQ41	D6	
Pod 6	Gnd	Gnd	A20	B20	Gnd	Gnd	Pod 6
(Even)	D9	DQ42	A21	B21	DM5	D8	(Even)
	D11	DQ46	A22	B22	DQ43	D10	
	Gnd	Gnd	A23	B23	Gnd	Gnd	
	D13	DQ48	A24	B24	DQ47	D12	
	D15	DQ52	A25	B25	DQ49	D14	
	Gnd	Gnd	A26	B26	Gnd	Gnd	
	Clk(-)	Gnd	A27	B27	DQ59	Clk(+)	

Bus and signal descriptions for J3

DQ Required.

DQS[3,4,5] Optional.

DQS8 Optional. No-connect if ECC is not used.

Connector J4: Data (double data rate)

Logic Analyzer		MPC85xx Signal	Soft Touch Pad #		MPC85xx Signal	Logic Analyzer	
	D1	DM6	A1	B1	DQ53	D0	
	D3	DQ54	A2	B2	DQS6	D2	
	Gnd	Gnd	A3	B3	Gnd	Gnd	
	D5	DQ55	A4	B4	DQ50	D4	
	D7	DQ60	A5	B5	DQ51	D6	Pod 7
Pod 7	Gnd	Gnd	A6	B6	Gnd	Gnd	(Odd)
(Odd)	D9	DQ61	A7	B7	DQ56	D8	
	D11	DM7	A8	B8	DQ57	D10	
	Gnd	Gnd	A9	B9	Gnd	Gnd	
	D13	DQ62	A10	B10	DQS7	D12	
	D15	DQ63	A11	B11	DQ58	D14	
	Gnd	Gnd	A12	B12	Gnd	Gnd	
	Clk(-)	No connect	A13	B13	No connect	Clk(+)	
	Gnd	Gnd	A14	B14	Gnd	Gnd	
	D1	ECC5 *	A15	B15	ECC4 *	D0	
	D3	ECC1 *	A16	B16	ECC0 *	D2	
	Gnd	Gnd	A17	B17	Gnd	Gnd	
	D5	ECC6 *	A18	B18	ECC2 *	D4	
	D7	ECC7 *	A19	B19	ECC3 *	D6	
Pod8	Gnd	Gnd	A20	B20	Gnd	Gnd	Pod 8
(Even)	D9	No connect	A21	B21	Trig_Out	D8	(Even)
	D11	MSRCID0	A22	B22	MSRCID1	D10	
	Gnd	Gnd	A23	B23	Gnd	Gnd	
	D13	MSRCID2	A24	B24	MSRCID3	D12	
	D15	MSRCID4	A25	B25	MDVAL	D14	
	Gnd	Gnd	A26	B26	Gnd	Gnd	
	Clk(-)	No connect	A27	B27	No connect	Clk(+)	

Bus and signal descriptions for J4

DQS[6,7] Optional.

ECC Optional. No-connect if ECC is not used.

MDVAL Optional but recommended.

MSRCID Optional but recommended.

To enable MSRCID[0:4] and MDVAL, MSRCID0 must be sampled low on POR (power-up, reset). (See Motorola's Reference Manual, section 20.4.3)

If you probe these signals, set the appropriate options in the DDR Bus Options dialog.

MSRCID[0:4] and MDVAL, if present:

- Eliminate the need for the user to specify instruction/data in the Memory Regions dialog.
- Allow the inverse assembler to inverse-assemble data cycles only, without the need for DDR command cycles to be collected by the trace analyzer.

Trig_Out Recommended.

DDR Connections for Soft Touch Pro Probing

Connector J1: Data (double data rate)

Logic Analyzer		Signal	Soft Touch Pad #		Signal	Logic Analyzer	
	D0	DQ0	A1	B1	Gnd	Gnd	
	D1	DQ4	A2	B2	DQ5	D2	
	Gnd	Gnd	A3	B3	DQ1	D3	
	D4	DQS0	A4	B4	Gnd	Gnd	
	D5	DM0	A5	B5	DQ2	D6	Pod 1
Pod 1	Gnd	Gnd	A6	B6	DQ6	D7	(Odd)
(Odd)	Clk(+)	No connect	A7	B7	Gnd	Gnd	
	Clk(-)	No connect	A8	B8	DQ7	D8	
	Gnd	Gnd	A9	B9	DQ3	D9	
	D10	DQ8	A10	B10	Gnd	Gnd	
	D11	DQ9	A11	B11	DQ12	D12	
	Gnd	Gnd	A12	B12	DQS1	D13	
	D14	DQ13	A13	B13	Gnd	Gnd	
	D15	DM1	A14	B14	DQ14	D0	
	Gnd	Gnd	A15	B15	DQ15	D1	
	D2	DQ10	A16	B16	Gnd	Gnd	
	D3	DQ11	A17	B17	DQ20	D4	
	Gnd	Gnd	A18	B18	DQ16	D5	
	D6	DQ17	A19	B19	Gnd	Gnd	
Pod 2	D7	DQS2	A20	B20	No connect	Clk(-)	Pod 2
(Even)	Gnd	Gnd	A21	B21	No connect	Clk(+)	(Even)
	D8	DQ21	A22	B22	Gnd	Gnd	
	D9	DM2	A23	B23	DQ18	D10	
	Gnd	Gnd	A24	B24	DQ22	D11	
	D12	DQ19	A25	B25	Gnd	Gnd	
	D13	DQ23	A26	B26	DQ24	D14	
	Gnd	Gnd	A27	B27	DQ28	D15	

See the bus and signal descriptions on page 22.

Connector J2: Address and control (single data rate)

Logic Analyzer		Signal	Soft Touch Pad #		Signal	Logic Analyzer	
	D0	No connect	A1	B1	Gnd	Gnd	
	D1	No connect	A2	B2	A0	D2	
	Gnd	Gnd	A3	B3	A1	D3	
	D4	A2	A4	B4	Gnd	Gnd	
	D5	A3	A5	B5	A4	D6	Pod 3
Pod 3	Gnd	Gnd	A6	B6	A5	D7	(Odd)
(Odd)	Clk(+)	No connect	A7	B7	Gnd	Gnd	
	Clk(-)	No connect	A8	B8	A6	D8	
	Gnd	Gnd	A9	B9	A7	D9	
	D10	A8	A10	B10	Gnd	Gnd	
	D11	A9	A11	B11	A10	D12	
	Gnd	Gnd	A12	B12	A11	D13	
	D14	A12	A13	B13	Gnd	Gnd	
	D15	A13	A14	B14	#RESET	D0	
	Gnd	Gnd	A15	B15	CKE1	D1	
	D2	CKE0	A16	B16	Gnd	Gnd	
	D3	No connect	A17	B17	BA1	D4	
	Gnd	Gnd	A18	B18	BA0	D5	
	D6	#RAS	A19	B19	Gnd	Gnd	
Pod 4	D7	#WE	A20	B20	#CK	Clk(-)	Pod 4
(Even)	Gnd	Gnd	A21	B21	CK	Clk(+)	(Even)
	D8	#CAS	A22	B22	Gnd	Gnd	
	D9	#CS0	A23	B23	#CS1	D10	
	Gnd	Gnd	A24	B24	#CS2	D11	
	D12	#CS3	A25	B25	Gnd	Gnd	
	D13	No connect	A26	B26	No connect	D14	
	Gnd	Gnd	A27	B27	No connect	D15	

See the bus and signal descriptions on page 23.

Connector J3: Data (double data rate)

Logic Analyzer		Signal	Soft Touch Pad #		Signal	Logic Analyzer	
	D0	DM4	A1	B1	Gnd	Gnd	
	D1	DQ25	A2	B2	DQ29	D2	
	Gnd	Gnd	A3	B3	DQS3	D3	
	D4	DM3	A4	B4	Gnd	Gnd	
	D5	DQ26	A5	B5	DQ30	D6	Pod 5
Pod 5	Gnd	Gnd	A6	B6	DQ27	D7	(Odd)
(Odd)	Clk(+)	DQ34	A7	B7	Gnd	Gnd	
	Clk(-)	Gnd	A8	B8	DQ31	D8	
	Gnd	Gnd	A9	B9	DQS8*	D9	
	D10	DM8	A10	B10	Gnd	Gnd	
	D11	DQ32	A11	B11	DQ36	D12	
	Gnd	Gnd	A12	B12	DQ33	D13	
	D14	DQ37	A13	B13	Gnd	Gnd	
	D15	DQS4	A14	B14	DQ38	D0	
	Gnd	Gnd	A15	B15	DQ39	D1	
	D2	DQ35	A16	B16	Gnd	Gnd	
	D3	DQ40	A17	B17	DQ44	D4	
	Gnd	Gnd	A18	B18	DQ45	D5	
	D6	DQ41	A19	B19	Gnd	Gnd	
Pod 6	D7	DQS5	A20	B20	Gnd	Clk(-)	Pod 6
(Even)	Gnd	Gnd	A21	B21	DQ59	Clk(+)	(Even)
	D8	DM5	A22	B22	Gnd	Gnd	
	D9	DQ42	A23	B23	DQ43	D10	
	Gnd	Gnd	A24	B24	DQ46	D11	
	D12	DQ47	A25	B25	Gnd	Gnd	
	D13	DQ48	A26	B26	DQ49	D14	
	Gnd	Gnd	A27	B27	DQ52	D15	

See the bus and signal descriptions on page 25.

Connector J4: Data (double data rate)

Logic Analyzer		Signal	Soft Touch Pad #		Signal	Logic Analyzer	
	D0	DQ53	A1	B1	Gnd	Gnd	
	D1	DM6	A2	B2	DQS6	D2	
	Gnd	Gnd	A3	B3	DQ54	D3	
	D4	DQ50	A4	B4	Gnd	Gnd	
	D5	DQ55	A5	B5	DQ51	D6	Pod 7
Pod 7	Gnd	Gnd	A6	B6	DQ60	D7	(Odd)
(Odd)	Clk(+)	No connect	A7	B7	Gnd	Gnd	
	Clk(-)	No connect	A8	B8	DQ56	D8	
	Gnd	Gnd	A9	B9	DQ61	D9	
	D10	DQ57	A10	B10	Gnd	Gnd	
	D11	DM7	A11	B11	DQS7	D12	
	Gnd	Gnd	A12	B12	DQ62	D13	
	D14	DQ58	A13	B13	Gnd	Gnd	
	D15	DQ63	A14	B14	ECC4*	D0	
	Gnd	Gnd	A15	B15	ECC5*	D1	
	D2	ECC0*	A16	B16	Gnd	Gnd	
	D3	ECC1*	A17	B17	ECC2*	D4	
	Gnd	Gnd	A18	B18	ECC6*	D5	
	D6	ECC3*	A19	B19	Gnd	Gnd	
Pod8	D7	ECC7*	A20	B20	No connect	Clk(-)	Pod 8
(Even)	Gnd	Gnd	A21	B21	No connect	Clk(+)	(Even)
	D8	Trig_Out	A22	B22	Gnd	Gnd	
	D9	No connect	A23	B23	MSRCID1	D10	
	Gnd	Gnd	A24	B24	MSRCID0	D11	
	D12	MSRCID3	A25	B25	Gnd	Gnd	
	D13	MSRCID2	A26	B26	MDVAL	D14	
	Gnd	Gnd	A27	B27	MSRCID4	D15	

See the bus and signal descriptions on page 26.

DDR Connections for FuturePlus Analysis Probes

The inverse assembler comes with configuration files to work with the FuturePlus analysis probes listed here:

Table 2 FuturePlus analysis probes

FuturePlus product number	Agilent product number*	Description
FS2331	FSI-60066	DDR333 SDRAM (The inverse assembler uses the analysis probe in "basic" mode. The analysis probe must be powered.)
FS2333	FSI-60081	DDR333 SO-DIMM
FS2336	FSI-60089	DDR400 DIMM basic

* Resale product number when ordered through Agilent

See Also

See the FuturePlus manuals for information on pin assignments and for instructions on connecting the analysis probe to your target system.

Information on analysis probes from FuturePlus can be found on the web at

http://www.futureplus.com

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